**Simulation Assignment #1**

**Simulation of Finite State Machine Designs**

In this assignment you will use digital logic simulation to verify the functionality of both the Mealy and the Moore Finite State Machine implementations of the Subtractor network that you developed in the Homework Assignment #1. You will use Verilog to model your design implementations as well as provide the input stimulus to your designs. You will develop both behavioral and structural models for your Mealy FSM implementation as well as a behavioral model for your Moore FSM implementation.

**Reference**

In this assignment you are required to use the ModelSim® Simulator to verify that three of the implementations of the two's complement serial subtractor works in a manner that implements the rules of multi-bit subtraction. To accomplish this, you are to create a separate *testbench* module that is used to drive each Subtractor implementation as the unit under test. A short guide for this is presented on the CPE 322 Canvas site and is entitled "[Simulating a Verilog HDL Design using the ModelSim® Compiler and Simulator in Stand-Alone Mode](https://uah.instructure.com/courses/59674/files/6009548?wrap=1)[Download Simulating a Verilog HDL Design using the ModelSim® Compiler and Simulator in Stand-Alone Mode](https://uah.instructure.com/courses/59674/files/6009548/download?download_frd=1)". To aid you in this process you can refer to the negator testbench example worked out in class under Homework & Simulations folder ([negator.v](https://uah.instructure.com/courses/59674/files/6135267?wrap=1" \t "_blank)[Download negator.v](https://uah.instructure.com/courses/59674/files/6135267/download?download_frd=1)and [tb\_negator.v](https://uah.instructure.com/courses/59674/files/6135268?wrap=1" \t "_blank)[Download tb\_negator.v](https://uah.instructure.com/courses/59674/files/6135268/download?download_frd=1))

**Assignment**

**Part 1: Behavioral Simulation of Mealy FSM using ModelSim™**

In this part of the assignment you are to simulate behaviorally the functionality of the State Graph (STG) of the Mealy FSM that you developed in Part 1 of Homework Assignment 1. You are to use the same input stimulus sequence that you developed in Part 1 of this homework assignment to verify that the design produces the correct results for this stimulus sequence. You are to simulate your design with ModelSim™ in the zero delay RTL mode.

This section of your report should include

* + a copy of the behavioral FSM Verilog Model of your design
  + a copy of your simulation testbench file
  + a screen shot of the waveform and the textual listing output that shows your simulation output. You should clearly indicate where you are applying each element of your input vector (**A** and **B**) and where you are monitoring your output (**D**) relative to the active edge of your clock.

**Part 2: Structural Simulation of Mealy FSM using ModelSim™**

In this part of the assignment you are to construct a structural model, in Verilog, of Part 2 of the Mealy FSM that you developed in Part 2 of Homework Assignment 1. You are to use again the same input stimulus sequence that you developed in Part 1 of this homework assignment to drive this version of your design in simulation. You are to simulate your design with ModelSim™  in the zero delay RTL mode.

This section of your report should include

* + a copy of your structural model of your gate-level implementation of your design
  + a copy of your simulation testbench file (which should be identical to the one used in Part 2 of this assignment).
  + a screen shot of the waveform and the textual listing output that shows your simulation output. You should clearly indicate where you are applying each element of your input vector (**A** and **B**) and where you are monitoring your output (**D**) relative to the active edge of your clock.

**Part 3: Behavioral Simulation of Moore FSM using ModelSim™**

In this part of the assignment you are to simulate behaviorally the functionality of the State Graph (STG) of the Moore FSM that you developed in Part 5 of Homework Assignment 1. You are to use the same input stimulus sequence that you developed in Part 1 of this homework assignment to verify that the design produces the correct results for this stimulus sequence. You are to simulate your design with ModelSim™ in the zero delay RTL mode.

This section of your report should include

* + a copy of the behavioral FSM Verilog Model of your design
  + a copy of your simulation testbench file (this should be based on you Moore version of your FSM design not the Mealy – so it will probably be different that the testbench file used in the other two parts)

a screen shot of the waveform and the textual listing output that shows your simulation output. You should clearly indicate where you are applying each element of your input vector (**A** and **B**) and where you are monitoring your output (**D**) relative to the active edge of your clock.